ELECTRODE CONFIGURATIONS FOR SEMICONDUCTOR DEVICES

TECHNICAL FIELD

[0001] This invention relates to semiconductor electronic devices, specifically devices with electrodes connected to field plates.

BACKGROUND

[0002] To date, modern power semiconductor diodes such as high-voltage P-I-N diodes, as well as power transistors such as power MOSFETs and Insulated Gate Bipolar Transistors (IGBT), have been typically fabricated with silicon (Si) semiconductor materials. More recently, silicon carbide (SiC) power devices have been researched due to their superior properties. III-Nitride (III-N) semiconductor devices are now emerging as an attractive candidate to carry large currents and support high voltages, and provide very low on resistance, high voltage device operation, and fast switching times. As used herein, the terms III-N or III-Nitride materials, layers, devices, etc., refer to a material or device comprised of a compound semiconductor material according to the stoichiometric formula $Al_xIn_yGa_zN$, where x+y+z is about 1.

[0003] Examples of III-N high electron mobility transistors (HEMTs) and III-N diodes, respectively, of the prior art are shown in FIGS. **1** and **2**. The III-N HEMT of FIG. **1** includes a substrate **10**, a III-N channel layer **11**, such as a layer of GaN, atop the substrate, and a III-N barrier layer **12**, such as a layer of $Al_xGa_{1-x}N$, atop the channel layer. A two-dimensional electron gas (2DEG) channel **19** is induced in the channel layer **11** near the interface between the channel layer **11** and the barrier layer **12**. Source and drain contacts **14** and **15**, respectively, form ohmic contacts to the 2DEG channel. Gate contact **16** modulates the portion of the 2DEG in the gate region, i.e., directly beneath gate contact **16**. The III-N diode of FIG. **2** includes similar III-N material layers to those of the III-N HEMT of FIG. **1**. However, the III-N diode of FIG. **2** only includes two contacts, an anode contact **27** and a cathode contact **28**. The anode contact **27** is formed on the III-N barrier layer **12**, and the cathode contact **28** is a single contact which contacts the 2DEG **19**. The anode contact **27** is a Schottky contact, and the single cathode contact **28** is an ohmic contact. In FIG. **2**, while there appears to be two cathode contacts, the two contacts are in fact electrically connected so as to form a single cathode contact **28**.

[0004] Field plates are commonly used in III-N devices to shape the electric field in the high-field region of the device in such a way that reduces the peak electric field and increases the device breakdown voltage, thereby allowing for higher voltage operation. An example of a field plated III-N HEMT of the prior art is shown in FIG. **3**. In addition to the layers included in the device of FIG. **1**, the device in FIG. **3** includes a field plate **18** which is connected to gate **16**, and an insulator layer **13**, such as a layer of SiN, is between the field plate and the III-N barrier layer **12**. Field plate **18** can include or be formed of the same material as gate **16**. Insulator layer **13** can act as a surface passivation layer, preventing or suppressing voltage fluctuations at the surface of the III-N material adjacent to insulator layer **13**.

[0005] Slant field plates have been shown to be particularly effective in reducing the peak electric field and increasing the breakdown voltage in III-N devices. A prior art III-N device similar to that of FIG. **3**, but with a slant field plate **24**, is shown in FIG. **4**. In this device, gate **16** and slant field plate **24** are formed of a single electrode **29**. Insulator layer **23**, which can be SiN, is an electrode-defining layer that contains a recess which defines at least in part the shape of electrode **29**. Electrode-defining layer **23** can also act as a surface passivation layer, preventing or suppressing voltage fluctuations at the surface of the III-N material adjacent to electrode-defining layer **23**. The gate **16** and slant field plate **24** in this device can be formed by first depositing electrode-defining layer **23** over the entire surface of III-N barrier layer **12**, then etching a recess through the electrode-defining layer **23** in the region containing gate **16**, the recess including a slanted sidewall **25**, and finally depositing electrode **29** at least in the recess and over the slanted sidewall **25**. Similar slant field plate structures can be formed in III-N diodes. For example, a III-N diode similar to that of FIG. **2** can also include a slant field plate connected to the anode contact **27**.

[0006] Slant field plates, such as field plate **24** in FIG. **4**, tend to spread the electric fields in the device over a larger volume as compared to conventional field plates, such as field plate **18** in FIG. **3**, which do not include a slanted portion. Hence, slant field plates tend to be more effective at reducing the peak electric field in the underlying device, thereby allowing for larger operating and breakdown voltages.

[0007] While slant field plates are desirable for many applications, they can be difficult to fabricate reproducibly. Field plate structures that can provide adequate suppression of peak electric fields and can be fabricated reproducibly are therefore desirable.

SUMMARY

[0008] In one aspect, a III-N semiconductor device is described that includes an electrode-defining layer having a thickness on a surface of a III-N material structure. The electrode-defining layer has a recess with a sidewall, the sidewall comprising a plurality of steps. A portion of the recess distal from the III-N material structure has a first width, and a portion of the recess proximal to the III-N material structure has a second width, the first width being larger than the second width. An electrode is in the recess, the electrode including an extending portion over the sidewall of the recess. A portion of the electrode-defining layer is between the extending portion and the III-N material structure. The sidewall forms an effective angle of about 40 degrees or less relative to the surface of the III-N material structure.

[0009] In another aspect, a III-N semiconductor device is described that includes an electrode-defining layer having a thickness on a surface of a III-N material structure. The electrode-defining layer has a recess with a sidewall, the sidewall comprising a plurality of steps. A portion of the recess distal from the III-N material structure has a first width, and a portion of the recess proximal to the III-N material structure has a second width, the first width being larger than the second width. An electrode is in the recess, the electrode including an extending portion over the sidewall of the recess. A portion of the electrode-defining layer is between the extending portion and the III-N material structure. At least one of the steps in the sidewall has a first surface that is substantially parallel to the surface of the III-N material structure and a second surface that is slanted, the second surface forming an angle of between 5 and 85 degrees with the surface of the III-N material structure.

[0010] Devices described herein may include one or more of the following features. The III-N material structure can